Silicon Meeting 6/30

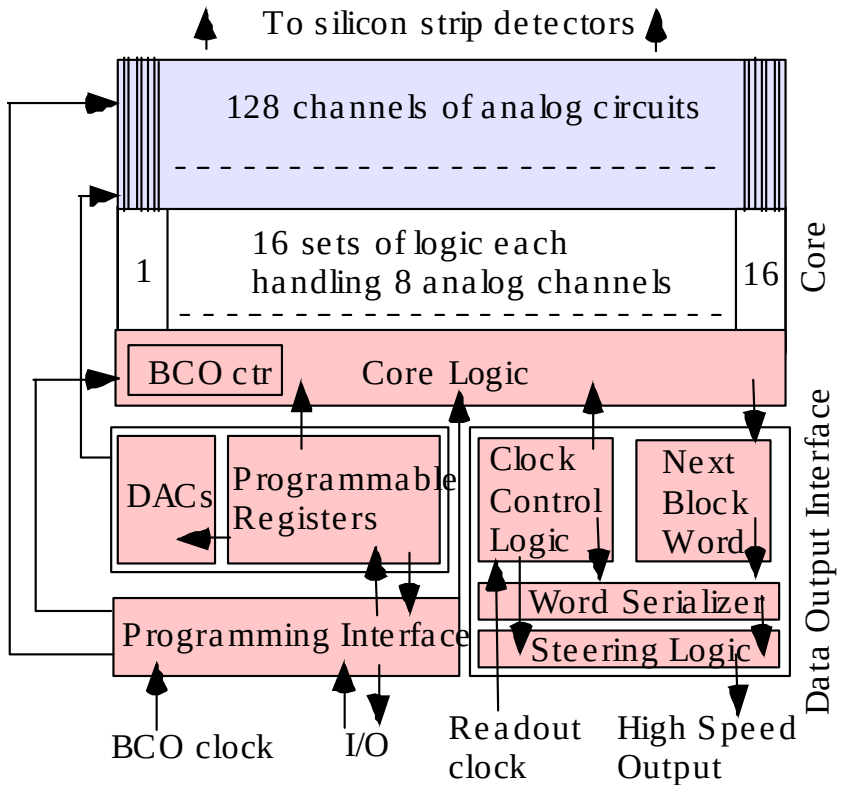
FNAL Update
LANL Lab Update
FNAL Pixel Contract
BNL Update
LANL Lab Near Term Plans

FNAL Update

- FSSR II came back
- Abder did his first test on May 5th to check the hang-up bug fix (ee tests) problem solved
- The Milano guys came beginning of June (physics group)
- I joined them in the week of June 6tha and we got the first new test board working.
- Returned with a test board, the DAQ software, the DAQ hardware, the firm ware, a firmware programmer (all at no cost)

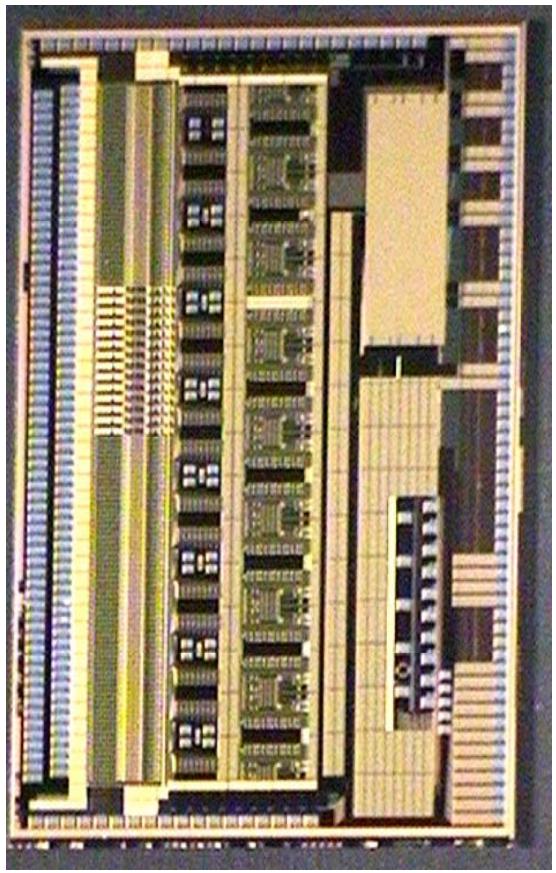
FSSR Block diagram

- FSSR Core
  - 128 analog channels
  - 16 sets of logic, each handling 8 channels
  - Core logic with BCO counter
- Programming Interface (slow control)
  - Programmable registers
  - DACs
- Data Output Interface
  - Communicates with core logic
  - Formats data output
  - Same as BTEV FPIX chip
    - Allows common DAQ



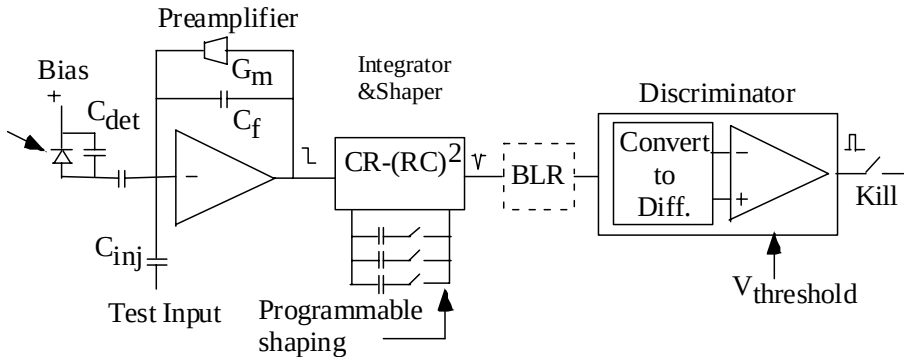
Chip Layout

- Chip has128 channels with all digital blocks
  - 50 micron pitch
  - Double row of bond pads
- Chip features for testing
  - One block of 64 channels has 32 with Baseline Restorer and 32 without
  - Different input transistor sizes were used on a few of the channels
  - A few of the analog front ends were removed to add multiple test points for adjacent channels
  - Individual transistors were added to characterize and compare their performance to operation in the preamplifier.
- Size is 7.27 mm x 4.46 mm



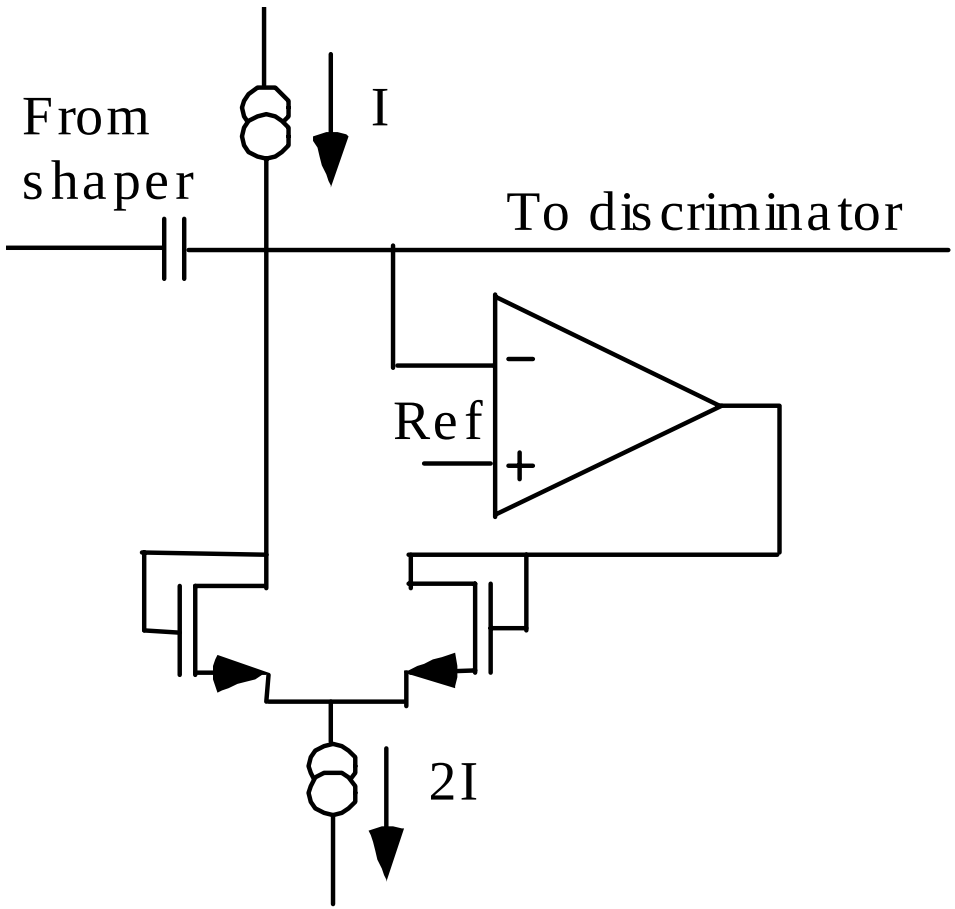
Analog Channels

- Preamplifier
  - Positive charge input
  - Gain of 5 mV/fC
- Integrator and shaper
  - CR-$(RC)^2$
  - Four programmable shaping times (65, 85, 105, 125 nsec)
- Base Line Restorer
  - Stabilizes base line
  - Blocks DC offset
  - Affects noise, threshold dispersion, gain (more info later)
- Discriminator
  - Comparator
  - Programmable threshold (chip wide)



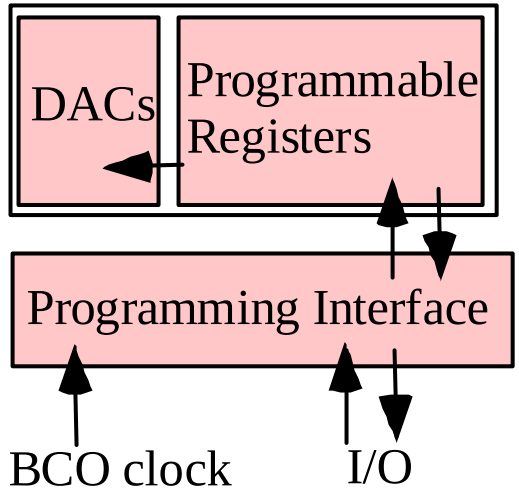
- 1 bit of 128 bit Serial shift register
  - Controls switch to provide Test Input
  - Controls switch to Kill discriminator output

Base Line Restorer Circuit



Digital Section

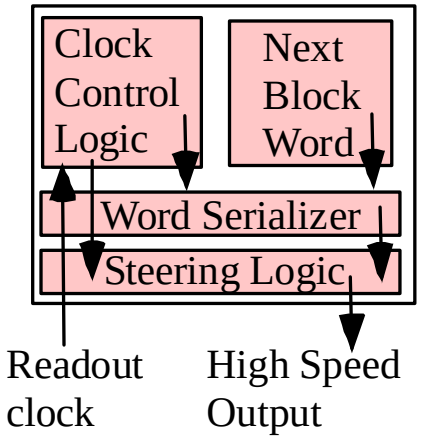
- Programming Interface
  - Receives 13 bit of serial data
    - 5 bits for chip ID
    - 5 bits for programmable address
      - CapSel – set shaping time
      - Kill – disconnect discriminator
      - Inject – control test pulse
      - AqBCO – store BCO value
      - Alines – select # of output serial lines
      - SendData – enable core
      - RejectHits – reject new hits
      - Three types of resets



- 3 bits for instructions
  - Write – download 2, 8, or 128 bits to register
  - Read – output bits in register
  - Set – set all register bits = 1
  - Reset – set all register bits =0
  - Default – set register bits to default value

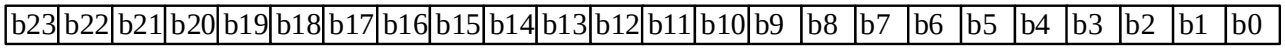
Digital Section (cont.)

- Data Output Interface
  - Serial data output
  - Number of output lines is programmable (1, 2, 4, 6)
  - LVDS output
  - No output buffering
  - Interfaces to Core Logic
  - Formats the data
  - Max data rate = 840 Mb/sec (6 lines)
  - Readout clock (70 MHz) independent of BCO clock
  - Data output is not time ordered

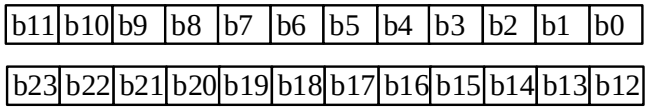


- Two types of 24 bit readout words
  - Sync/Status
    - 10 bits status
    - 13 bits for synchronization
    - 1 bit for word mark
  - Data word
    - 4 bits for strip number (1 of 8)
    - 5 bits for logic set number
    - 8 bits for hit BCO number
    - 6 bits are currently unused

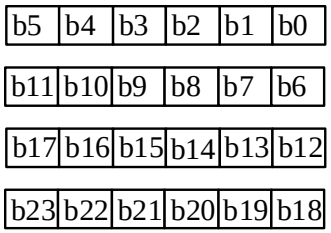
Output Data Format



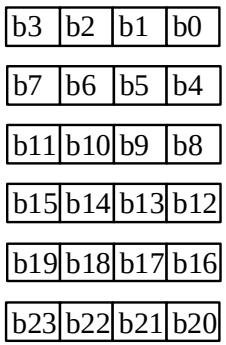
(a) One output pair



(b) Two output pairs



(c) Four output pairs



(d) Six output pairs

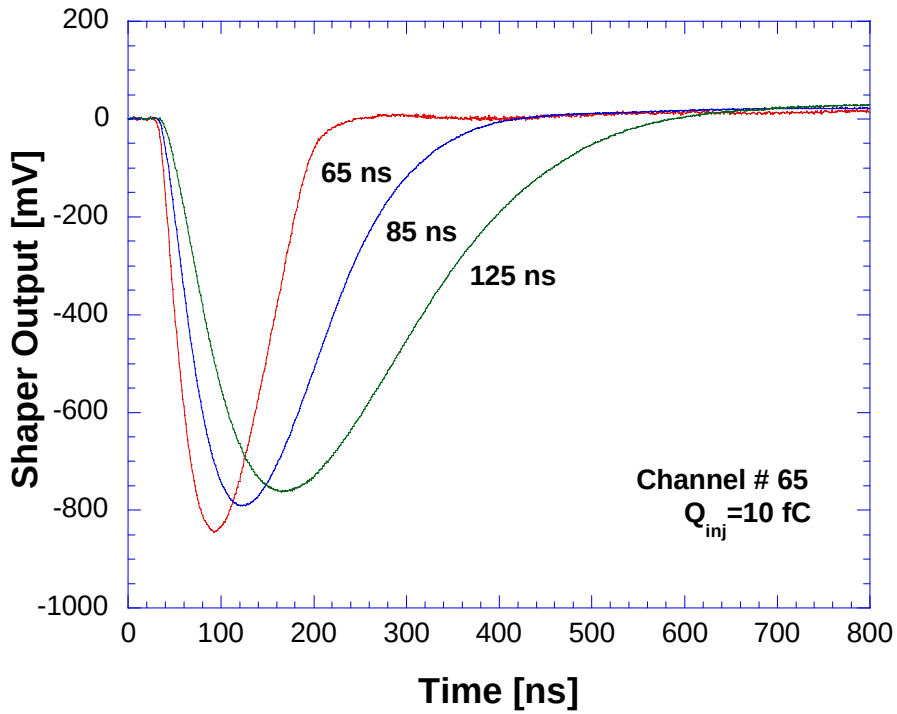
Readout speed depends on number of lines used

FSSR I - Test Results

- The analog and digital sections along with all test structures functioned properly allowing extensive testing of the chip.
- Noise performance is close to predicted values.
- Overall gain is about 80 mV/fC.
- Wide dynamic range of about 12 fC
- Power dissipation is 3 mW/channel
- The chip has been operated operated with a 70 MHz readout clock to provide 840 Mb output data rate.
- Threshold dispersion = 440 erms (with BLR)
- ENC (C_{det} = 20 pF, shaping time = 125 nsec, with BLR) is 790 erms.
- All specifications met but readout hangs under certain conditions

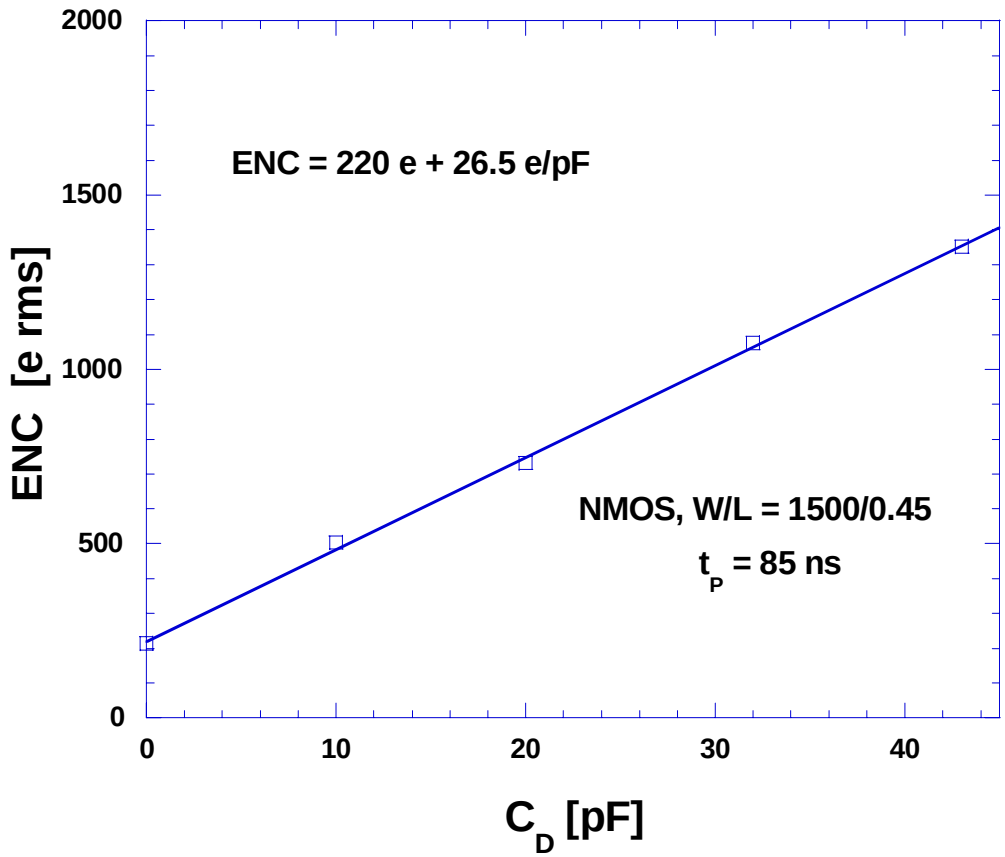
Averaged Waveforms at Shaper Output Showing Different Shaping Time Settings

- Shaping time can be programmed (65, 85, 105, 125 nsec)
- Adjustment allows for
  - Foundry process variations
  - Different beam interaction times.
- Has small tail lasting for several microseconds that might cause a problem.



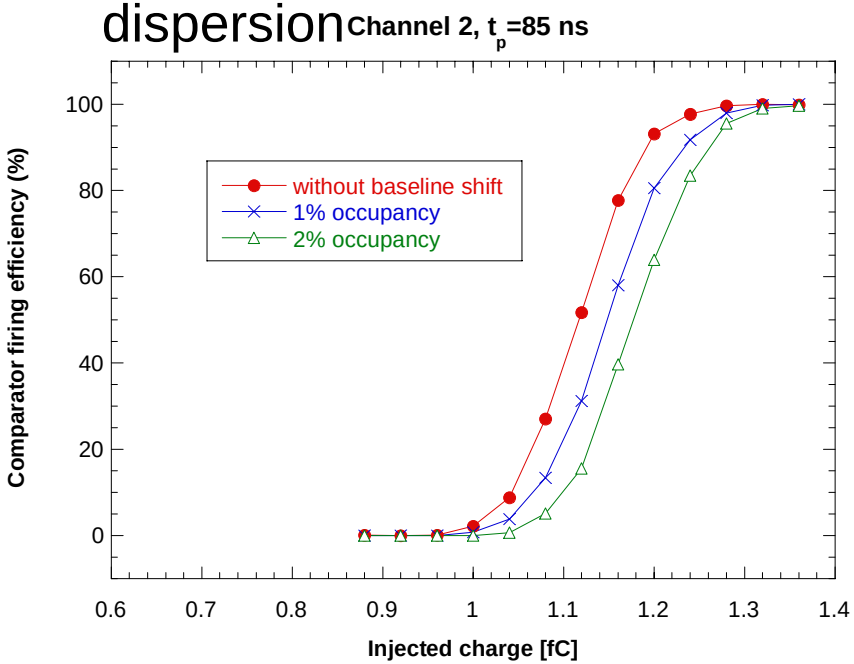
Equivalent Noise Charge Measurement at Shaper Output

- Close to simulated value
- Noise depends on shaping time

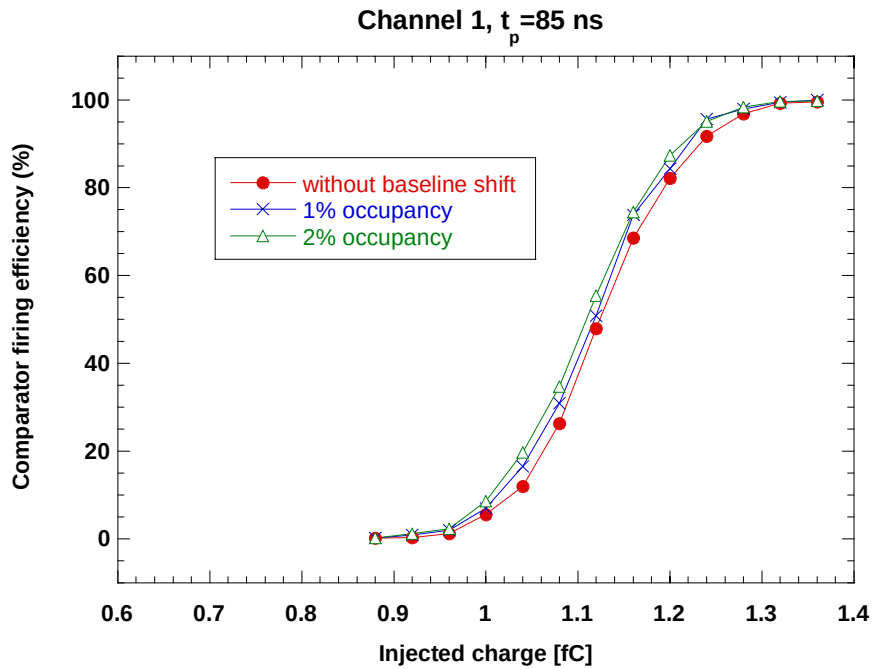


Base Line Restorer Test Results

- Shaper output has small overshoot.
- Overshoot causes unwanted variable offset at discriminator input.
- BLR removes variable offset.
- BLR also improves threshold dispersion (AC coupling), but increases noise.
- BLR is needed to remove variable offset and improve threshold dispersion



Input signal discriminator scan without BLR



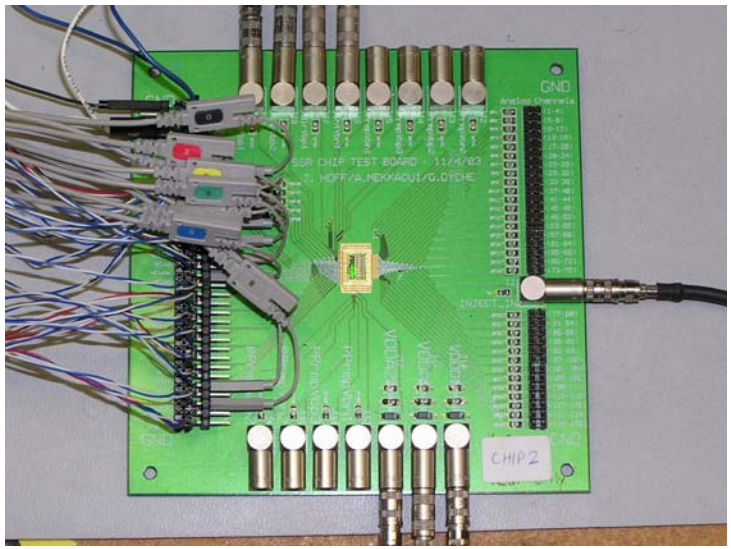
Input signal discriminator scan with BLR

FSSR II Changes

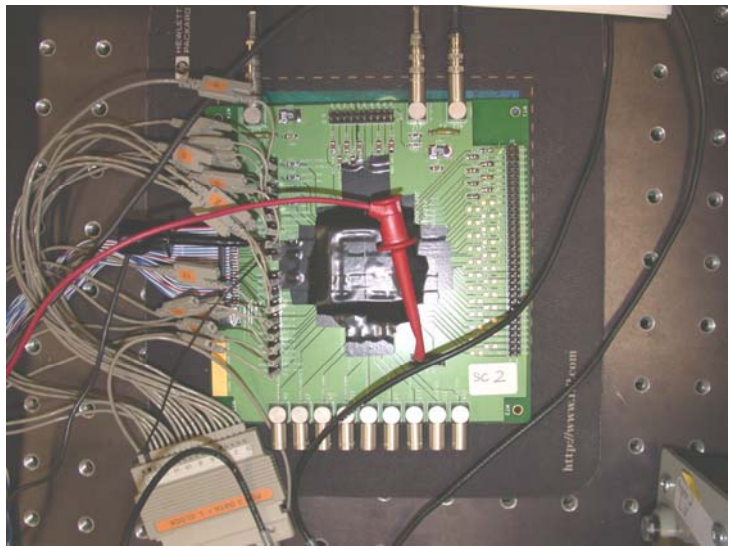
- Since the current chip has unnecessarily wide dynamic range, the gain will be increased by decreasing the size of the preamplifier feedback capacitor from 200 fF to 150/100 fF. This will cause a further reduction in threshold dispersion.
- It was recently decided that a simple discriminator output will not satisfy the need to calibrate the detector as radiation changes its characteristics.
  - A 3 bit ADC, similar to the one used in the BTEV FPIX chip, will be added to each channel– considered low risk.
  - The 3 bits will be inserted into the data word to replace 3 of the 6 unused bits. Thus there is no impact on the data rate.

FNAL Details

old



new

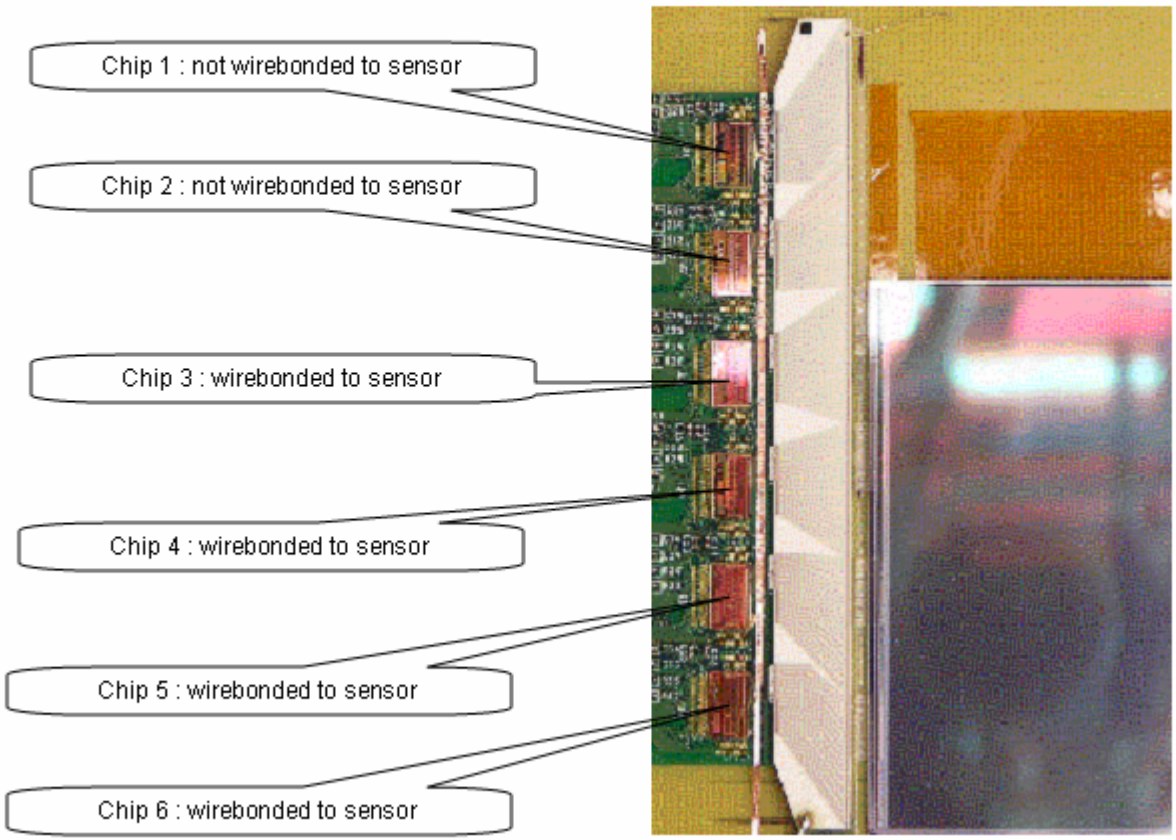


- FSSR 2 has a new connection layout
  - No hardware from FSSR 1 works directly
  - First test with patched (*spaghetti bowl* bonding) single chip board
  - New Testboard by Cardoso in early June.

The Hybrid Board and Sensor

Configuration

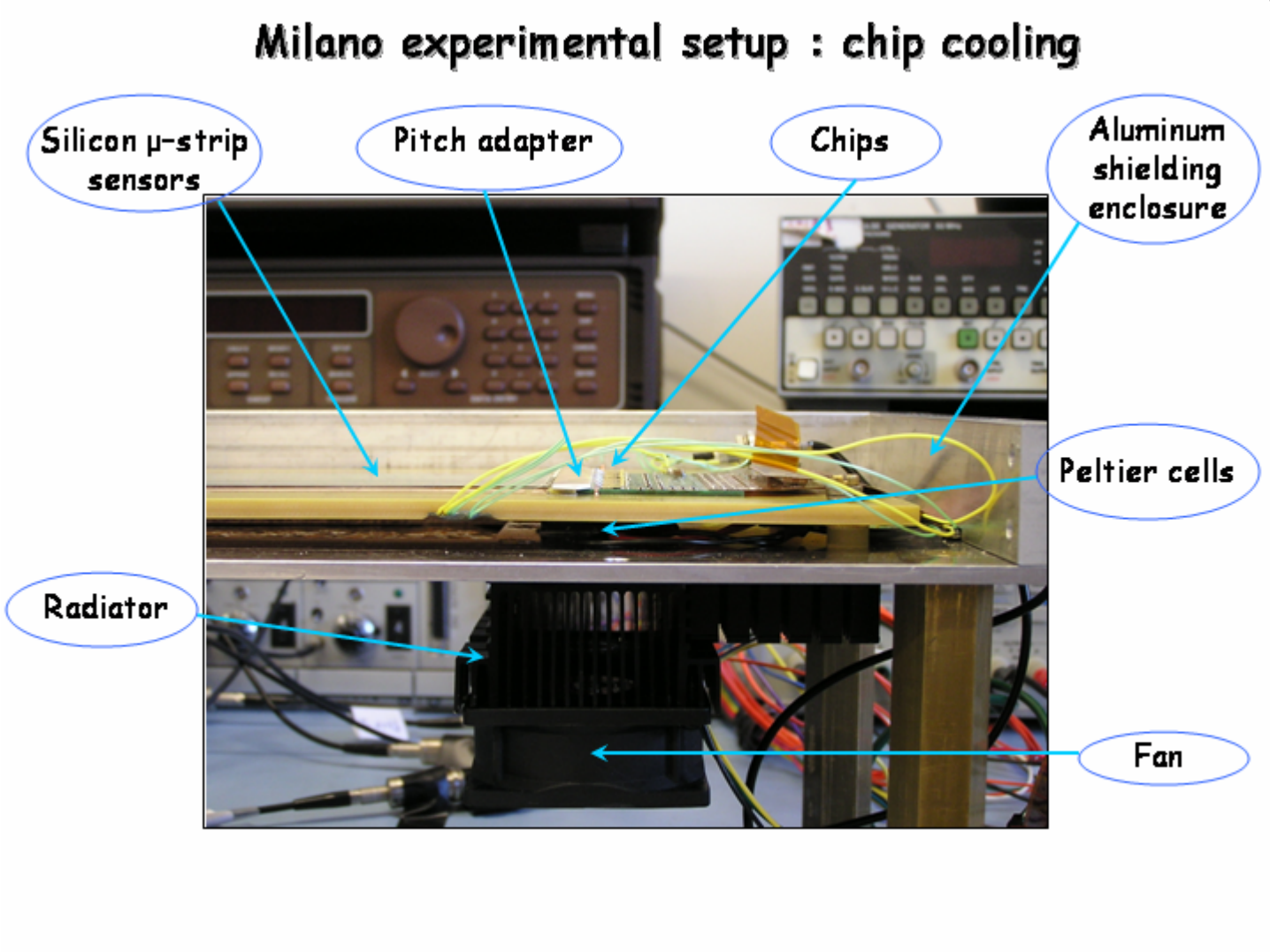
Array of 6 chips



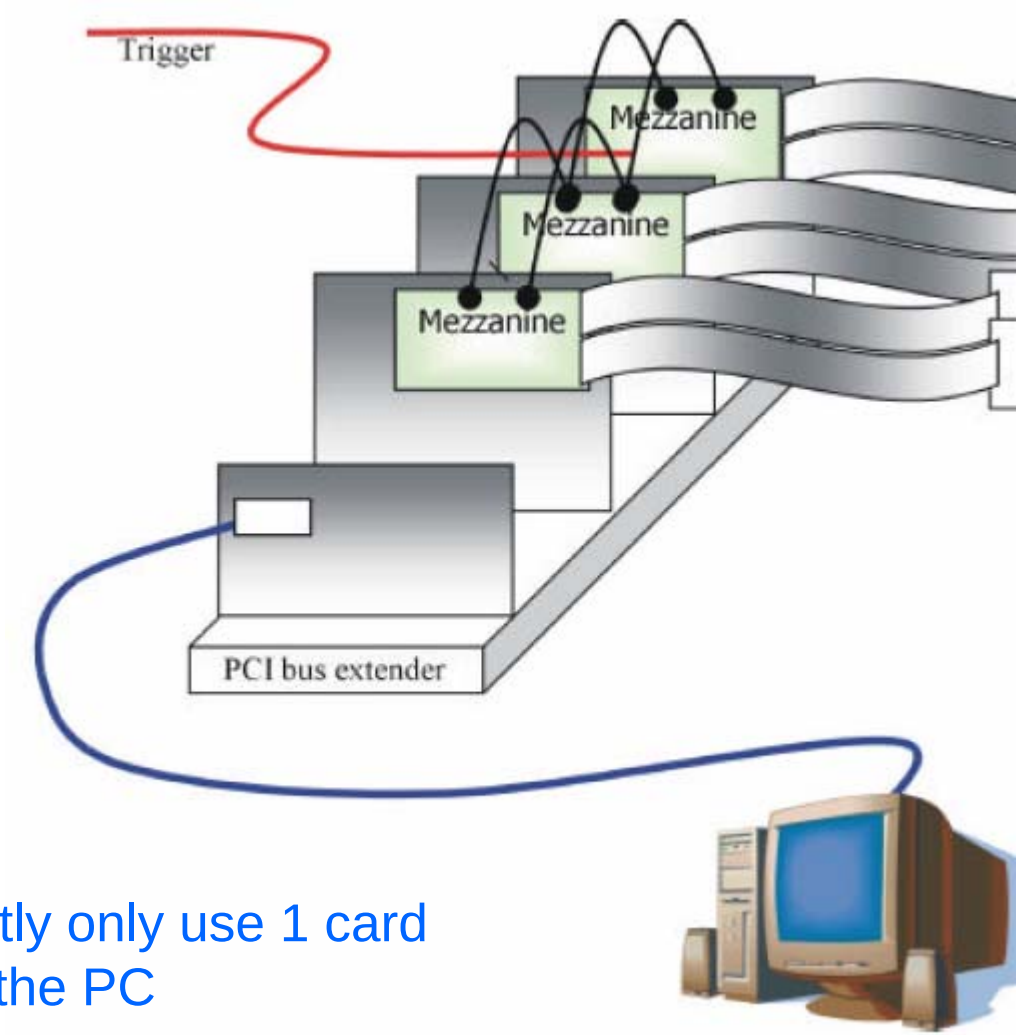
The HDI and Adapter

- 200 line HDI to a board with pluggable connectors

Cooling is solved via Peltier elements for multi chip boards



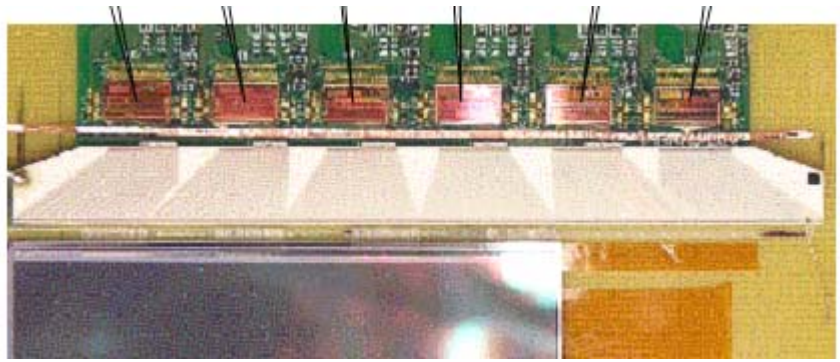
Multi Card Test Stand



We currently only use 1 card directly in the PC

Agreement with G. Cardoso

- We will get one or two hybrid boards in July with 6 FSSR II wire bonded to strip detectors either we or them provide !



LANL Lab Update

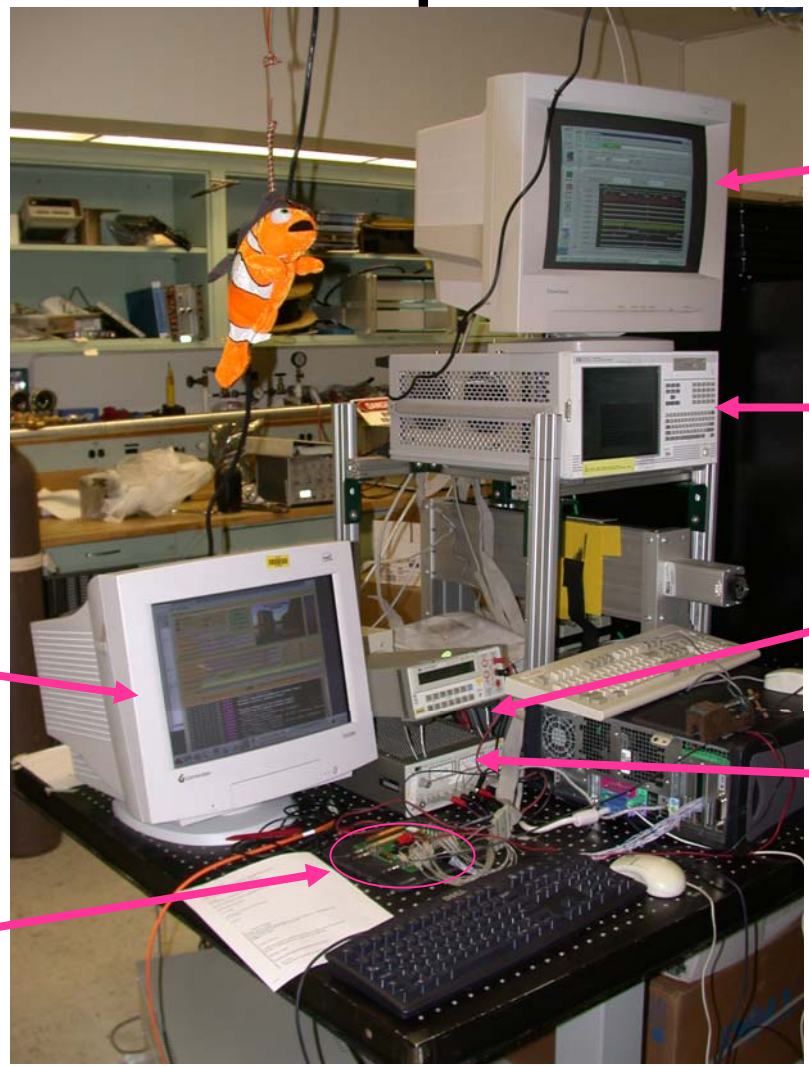
- We are setup in C129 to work with the FSSR
- We can program and read out the chip
- The chip has a single channel were one can see with the scope the signal after shaper, baseline restorer etc.
- We are ready to do noise and speed measurements even add an actual silicon detector for input

Were we are ☺

C129

- You need Rad Worker II and extra course
- Radioactive Sealed Source custodians and users shall complete the on-line Sealed Source Safety, Self-Study Course #15907. Compliance requirements LIG 402-718-01 Section 3.5. Pre-requisites Radiological Worker II Exam Course #12909. Length approximately 4 hours.

We have what we need in the Compton Lab



LA Display

Logic Analyzer

DVM

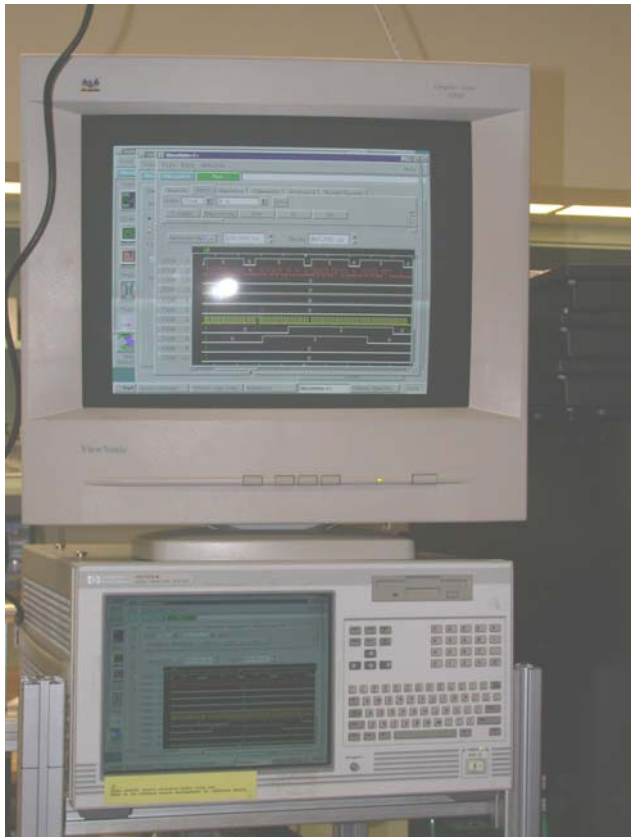
DAQ

Low Voltage

Test Board

Invisible: Clean Power and Scope and Pulser

We have a HP Logic Analyzer



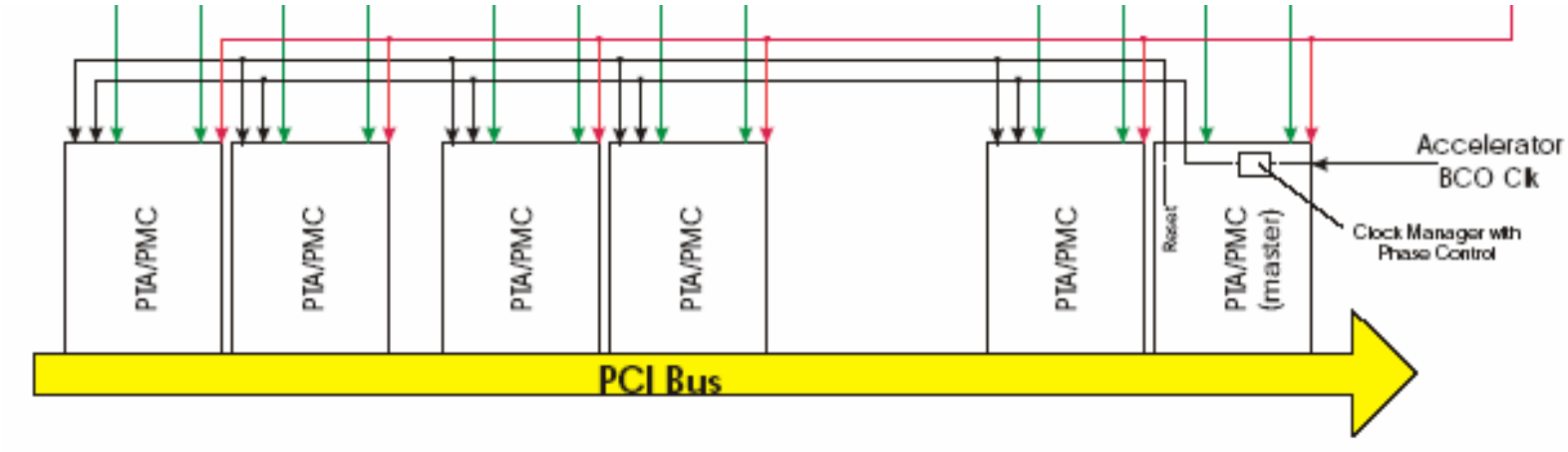
We need to build up a pool of people who know how to operate this rather complex tool !

Here are the links to the manuals:

http://cp.literature.agilent.com/litweb/pdf/5988-9058EN.pdf

http://cp.literature.agilent.com/litweb/pdf/5988-9023EN.pdf

DAQ



- PTA card on PCI bus
  - PCI Test Adapter
- PMC card to talk to hybrid
  - Programmable Mezzanine card
- Linux based system
- Well documented POMONE software
  - http://cuf.mi.infn.it/pomone/html/index.html

PCI-Cards have FPGAs

PTA

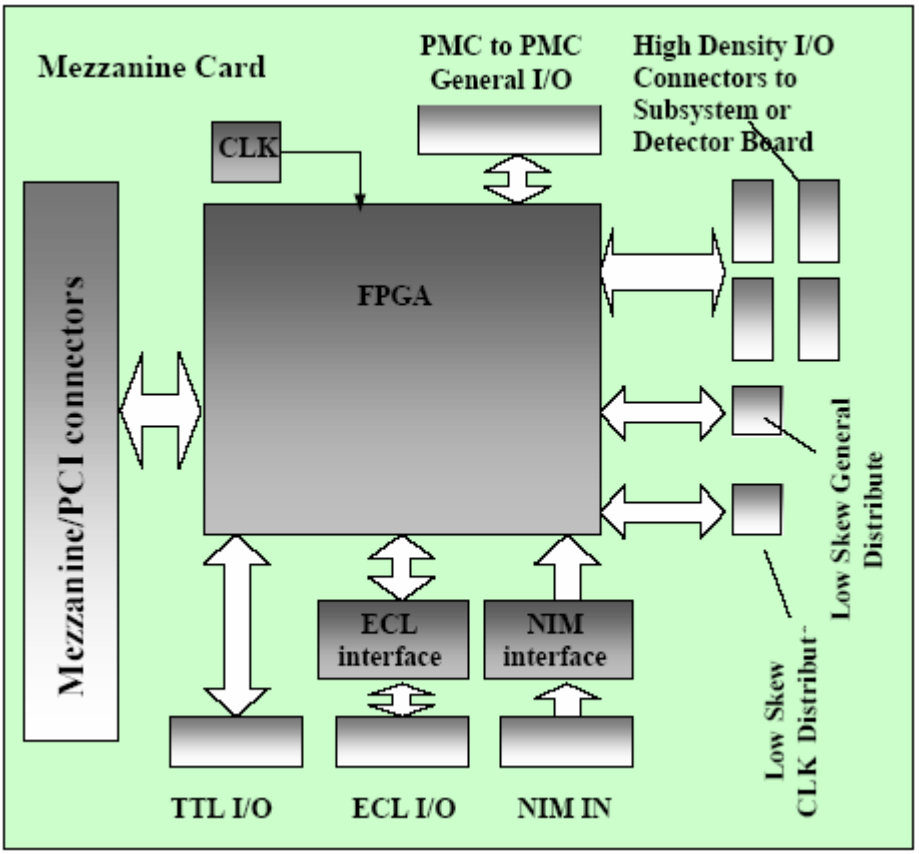
PMC

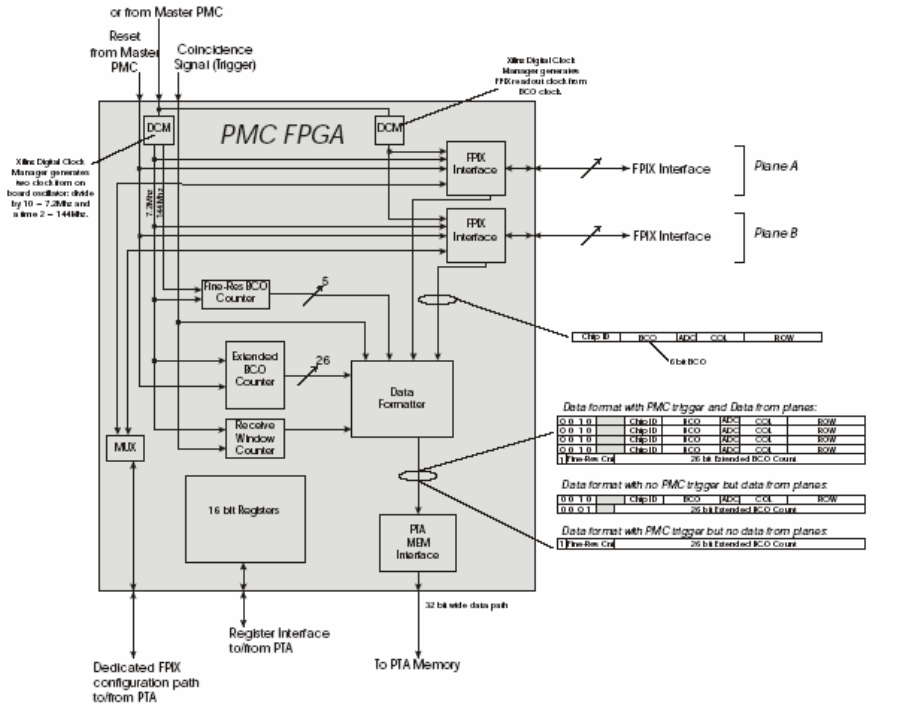
Firmware programming jack

Programmable Test Adapter is generic

Programmable Mezzanine Card is specific

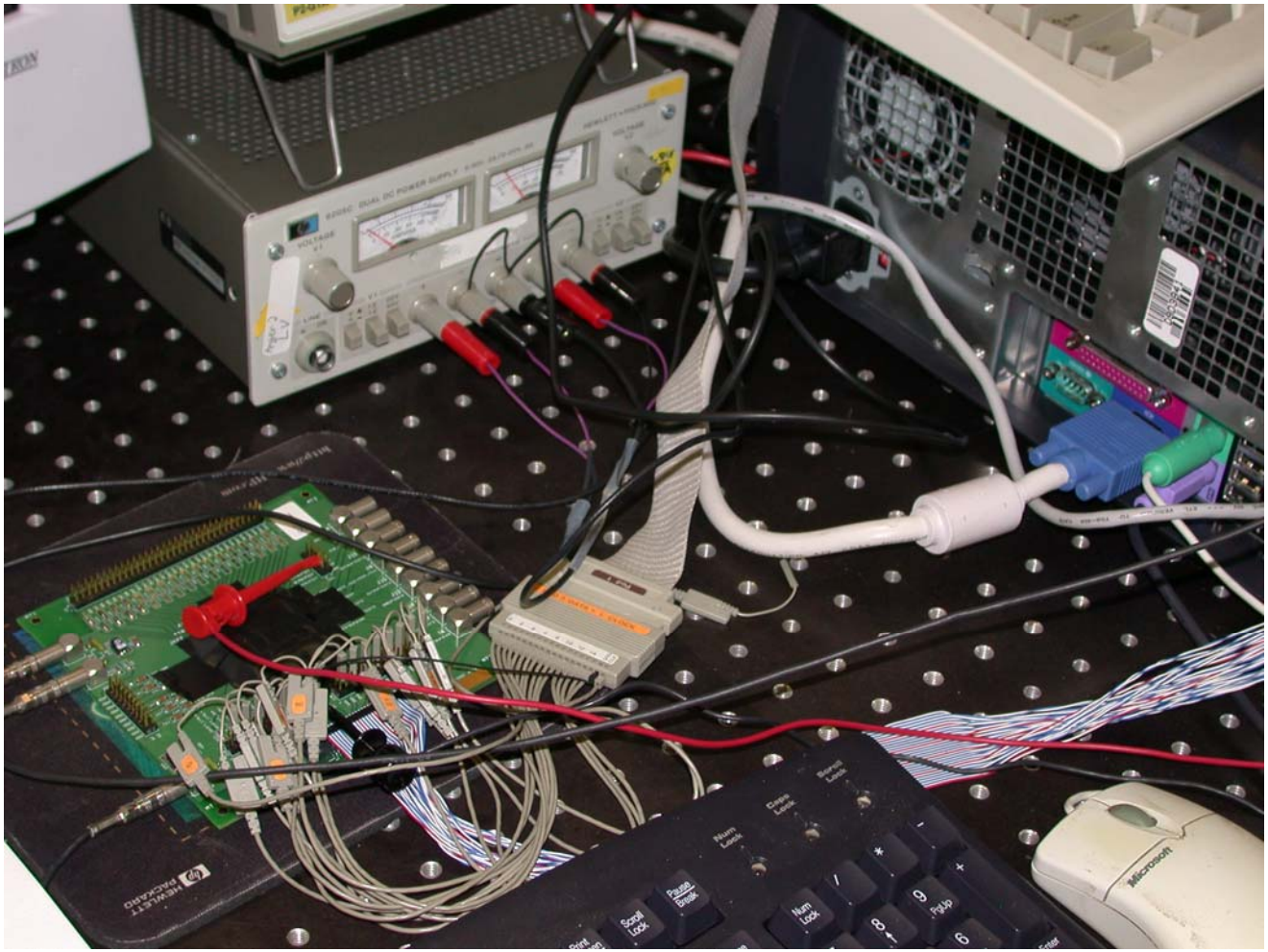
Programmable Mezzanine Card





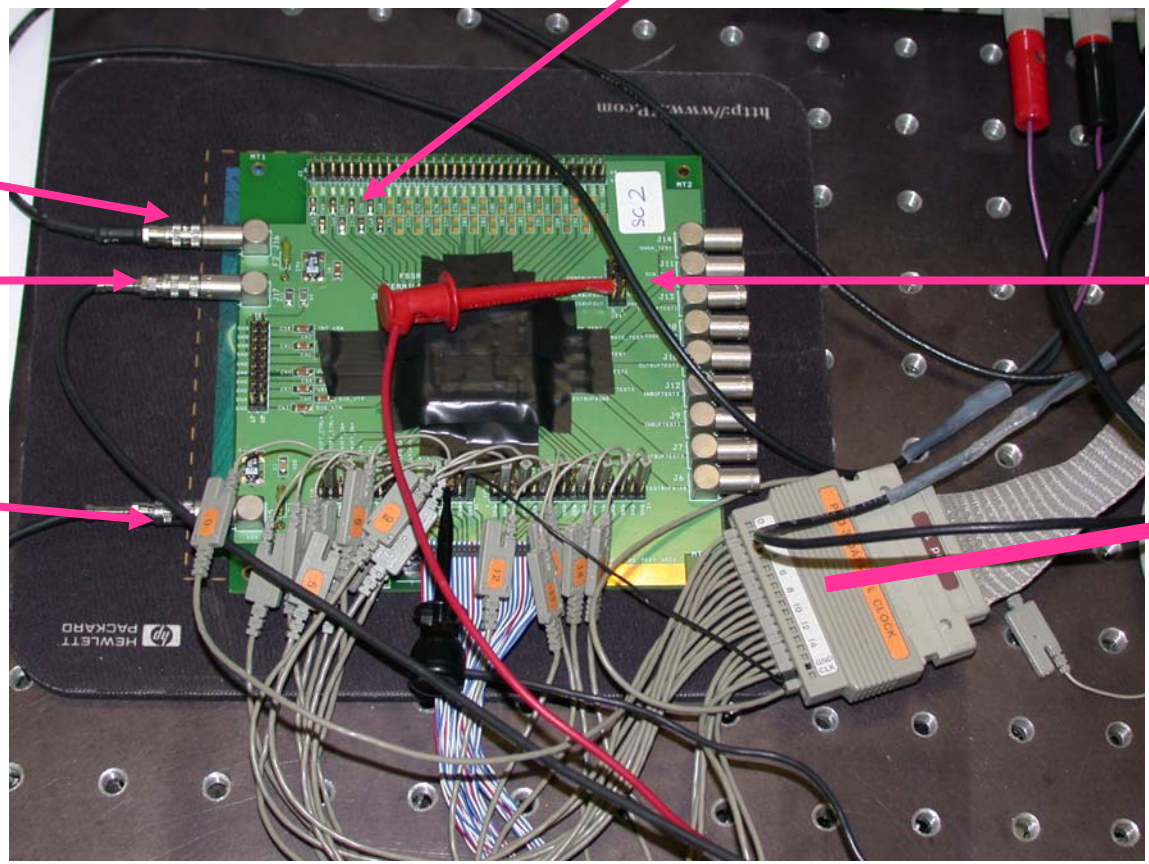
We have Xilinx freeware to program the FPGA but not to edit firmware, Chuck will buy the license for us

Close-up of Setup



The FSSR II Test Board

32 input lines, some have capacitors for noise measurement

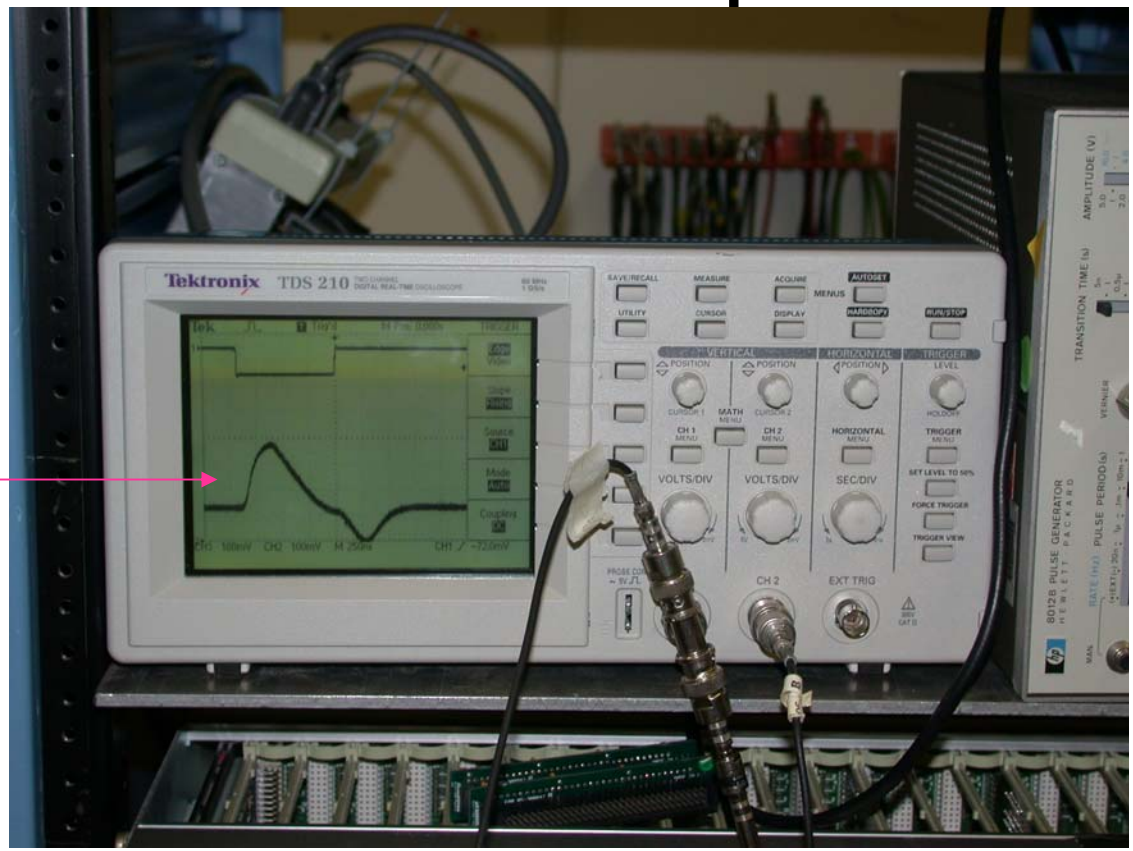


LVDS bus signals from the PCM

We can enable pulser in DAQcfg.xml to look at one analog signal with the scope

Pulser 1 Volt DC offset, 200 mV pulse

Shaper response




```
</Pulser>
        <Cell Inj="YES" Comment="" Row="7" Kill="NO" Col="15" />
      </Detector>
```

LANL Summary

- We are ready to measure !
- Need to build expertise
  - HP Logic Analyzer
  - Xilinx Programming
  - POMONE DAQ Software
  - Noise Measurements
  - Etc ..
- Should discuss laser vs. electron gun ..

LANL-FNAL Pixel Contract

- FNAL submitted a new version of the FPIX II, there was not enough money for a FPIX III
  - No pulser but fixed readout bug, new analog front-end to handle leakage current better
- D. Christian proposes that for ~35-40k we get multichip FPIX assemblies bumpbonded to detectors and mounted on HDIs … either 5/6 or 8 chip modules plus new readout hardware
  - Available in January if we move now !
  - My preferred solution for DR-Detector (separate discussion)
  - The EE who did the HDIs will come soon to visit LANL

BNL Summary

- On June 15th I met with O'Brien, Chi, Haggerty, Lajoie, Akiba and Craig to discuss the 'data push' idea
  - Positive experience
    - Haggerty asked why we don't do the whole VTX like that ?
- O'Brien send email summary and to do list

  - I (Ed) think that we had a useful meeting last week on the FVTX electronics. At least I could begin to understand some of the performance characteristics of the proposed electronics. It is clear that there is considerable work to do before we can define how a chip in the PHX/BTeV family of electronics can be interfaced with the PHENIX DAQ. We first need a conceptual design of all components, lets call them circuit boards, in the electronics chain, and next we need a spec sheet for each of these circuit boards describing their functionality.

Summary

- We need people to actively join the effort
- Need to decide on the FPIX contract before mid July
- Need to work on Ed's list

- Go to p25ext.lanl.gov/~kunde for links and information …